REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed July 23, 2008. The Examiner is thanked for the thorough examination of the present application. Upon entry of this response, claims 1-6, 13-24 and 32-38 are pending in the present application. Applicants respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Response to Claim Objections

Applicants have canceled claims 15 and 34, thereby rendering the claim objections moot.

II. Response to Claim Rejections Under 35 U.S.C. § 112

On page 2, the Office Action alleges that with independent claims 13 and 32, it is unclear how the claimed embodiments reduce the number of processor cycles since nothing within the claims relate to the processor cycles. As indicated above, Applicants have amended claims 13 and 32 to address the §112, 2nd paragraph rejections. Accordingly, Applicants respectfully request that the rejections be withdrawn.

III. Response to Claim Rejections Under 35 U.S.C. § 101

On page 3, the Office Action alleges that claims 1-6 and 20-24 merely disclose a series of mental steps/components for determining a minimum/maximum value among values without disclosing a practical/physical application. Applicants respectfully disagree. Independent claims 1 and 20 are both directed to a processor.

Furthermore, the claims clearly recite various structural features (*e.g.*, destination register, source register). As such, Applicants respectfully submit that these claims are directed to more than just a series of mental steps. Moreover, one of ordinary skill in the art would appreciate that the structural components recited in these claims (*e.g.*, registers) are not abstract components but instead are components that may be embodied in hardware or software executed by a processor (or a combination thereof). Applicants respectfully submit that registers, for example, may be considered to be an "articles of manufacture" or "machines", which are explicitly recognized as statutory subject matter under §101. Accordingly, Applicants respectfully request that the rejection be withdrawn.

IV. Response to Claim Rejections Under 35 U.S.C. § 102

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102.

Claims 13-15 and 32-34 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by *Okumura et al.* (U.S. Pat. No. 5,726,923, hereinafter "*Okumura*"). For at least the reasons set forth below, Applicants traverse these rejections.

A. Independent Claim 13

Applicants respectfully submit that independent claim 13 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the features emphasized below in claim 13.

Claim 13, as amended, recites (emphasis added):

> 13. A method for reducing a number of processor cycles for determining a minimum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:
>
> ***assigning a destination register with an index value and a value of a first source register from among the plurality of source registers***;
>
> for each of the plurality of source registers,
>
> comparing a value stored in the source register with a value stored in a destination register;
>
> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is less than the value stored in the destination register; and
>
> wherein comparing, concatenating, and storing are implemented by a single processor instruction and performed within a single processor cycle.

Applicants have amended claim 13 and submit that no new matter is added. In alleging that *Okumura* discloses the feature emphasized above, the Office Action states the following:

> *"Figure 2 as general data structure of each specific registers 11x in Figure 4 as repeated loop. Within the next repeated loop, the initial/stored register has the content of the previous loop which is the index value and the value of the first source register."*

(Office Action, page 4). Applicants respectfully disagree with the statement that "within the next repeated loop, the initial/stored register has the content of the previous loop which is the index value and the value of the first source register." *Okumura* is directed

to a minimum/maximum data detector for rapidly detecting the minimum or the maximum data from a plurality of numeric data. Further, *Okumura* states, "once the read out of one series of consecutive numeric data have been completed, then the numeric data remaining in the specific register 11 is the minimum data. The address of the minimum data in the memory 1 can be obtained by adding the index (counted results) and the top address utilized at the beginning of the detection." (*Okumura*, Abstract). The specific register 11 contains the minimum data, but this does not necessarily correlate with the "first source register," as alleged by the Office Action. As such, Applicants respectfully submit that *Okumura* fails to disclose "assigning a destination register with an index value and a value of a first source register from among the plurality of source registers" as recited in claim 13.

Accordingly, Applicants respectfully submit that independent claim 13 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the highlighted features in claim 13 above.

B. Independent Claim 32

Applicants respectfully submit that independent claim 32 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the features emphasized below in claim 32.

Claim 32, as amended recites (emphasis added):

> 32. A method for reducing a number of processor cycles for determining a maximum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:

> ***assigning a destination register with an index value and a value of a first source register from among the plurality of source registers***;
> for each of the plurality of source registers,
> comparing a value stored in the source register with a value stored in a destination register;
> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is greater than the value stored in the destination register; and
> wherein comparing, concatenating, and storing are performed within a single processor cycle.

While claims 32 and 13 are not coextensive in scope, Applicants rely on arguments similar to those expressed above for claim 13. (Moreover, the Office Action relies on the same arguments set forth in rejecting claim 13 to reject claim 32.) *Okumura* states that the operations described are used for detecting the minimum data, but that maximum data can be detected in the same way. As such, the specific register 11 contains the minimum/maximum data, but this does not necessarily correlate with the "first source register," as alleged by the Office Action. As such, Applicants respectfully submit that *Okumura* fails to disclose "assigning a destination register with an index value and a value of a first source register from among the plurality of source registers" as recited in claim 32.

Accordingly, Applicants respectfully submit that independent claim 32 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the highlighted features in claim 32 above. Furthermore, Applicants submit that dependent claim 33 is allowable for at least the reason that this claim depends from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

V. Response to Claim Rejections Under 35 U.S.C. § 103

The USPTO has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP §2141, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

For a proper rejection of the claim under 35 U.S.C. §103, the cited combination of references must disclose, teach, or suggest all elements / features of the claim at issue. See, e.g., *In re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Claims 1-6 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Okumura*. Claims 16-19 and 35-38 are rejected as being unpatentable over *Okumura* in view of the admitted prior art. For at least the reasons set forth below, Applicants traverse the rejections set forth.

A. Independent Claim 1

Applicants respectfully submit that independent claim 1 patently defines over *Okumura* in view of the admitted prior art for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 1.

Claim 1 recites (emphasis added):

> 1. A processor for reducing the processing effort for determining a minimum value of a plurality of values stored in source registers and determining an index value of a source register having the minimum value, the processor comprising:
> a destination register;

a first source register storing a first value, wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register;

a second source register storing a second value, wherein the second source register comprises S bits, and wherein the second value comprises N lower bits of the second source register;

means for comparing the first value stored in the first source register with the second value stored in the second source register;

means for storing the first value in the destination register ***when the first value is less than or equal to the second value***; and

means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register ***when the second value is less than the first value***, wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value.

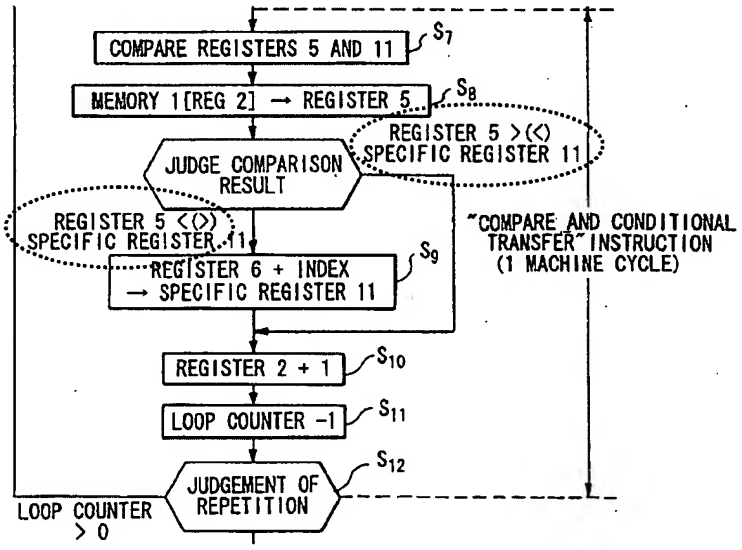
The Office Action continues to allege that the *Okumura* reference discloses each of the features recited in claim 1. In the Response to Arguments section, the Office Action states that Applicants' arguments are considered moot in view of the new grounds of rejection. The Office Action, however, sets forth substantially the same rejections with respect to claim 1. Applicants respectfully traverse the rejection and submit that *Okumura* fails to disclose all the features in claim 1.

Before addressing the rejection in view of *Okumura*, Applicants would like to emphasize that claim 1 recites various components for handling the first or second value based on the outcome of the comparison conducted between these values. In particular, the claim language clearly addresses two conditions – 1) when the first value is less than or equal to the second value; AND 2) when the second value is less than the first value. Claim 1 clearly recites components for performing certain actions based on these conditions. As such, claim 1 recites means for performing certain steps for both conditions.

Referring now to the *Okumura* reference, the Examiner makes the following correlations:

Claim 1	***Okumura***
a first source register storing a first value	specific register 11
second source register storing a second value	registers 5-6
destination register	specific register 11
index value	index field 11b

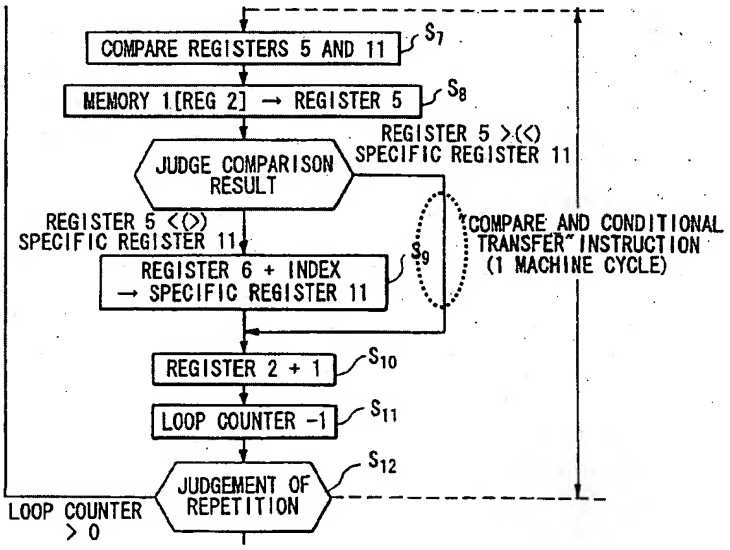
(*See* Office Action, page 6). With reference to FIG. 3 in *Okumura*, if the content of register 5 (allegedly the "second source register" in claim 1) is judged to be less than the content of the specific register 11 (allegedly the "first source register" in claim 1), step S9 is executed. This is depicted in the "compare and conditional transfer" section in FIG. 3 below:



In step S9, the content of register 6 and the counted result of the counter 9 are "linked" in the index linking circuit 10, and the linked result is stored in the specific register 11. At most, however, this correlates with "means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register *when the second value is less than the first value*, wherein the index

value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value."

Okumura, however, fails to teach of storing the first value in the destination register *when the first value is less than or equal to the second value*. Reference is made to the related text for steps S7-S9 in FIG. 3 of *Okumura*. If the content of register 5 (allegedly the "second source register" in claim 1) is judged to be larger than or equal to the content of the specific register 11 (allegedly the "first source register" in claim 1), *Okumura* only teaches that step S9 is not executed or bypassed. (See "Judge Comparison Result" block.) This corresponds to the "*path of specific register 11 less than register 5*" as set forth in the Office Action. (Office Action, page 6).



Okumura does not teach of storing the first value (specific register 11) in the destination register (specific register 11) when the first value (specific register 11) is less than or equal to the second value (registers 5-6). (See steps S10, S11.) Claim 1 explicitly recites: 1) means for storing the first value in the destination register when the first value is less than or equal to the second value; and 2) means for concatenating the index

value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is less than the first value. *Okumura* fails to disclose both of these features in the cited text/figure. In particular, *Okumura* fails to disclose (means for) "storing the first value in the destination register when the first value is less than or equal to the second value." While Applicants appreciate the fact that FIG. 3 in *Okumura* shows that the comparison can be reversed (*i.e.*, "< (>)"), *Okumura* nevertheless fails to disclose each of the elements in claim 1.

Accordingly, Applicants respectfully submit that independent claim 1 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the highlighted features in claim 1 above. Furthermore, Applicants submit that dependent claims 2-6 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

B. Independent Claim 17

Applicants respectfully submit that independent claim 17 patently defines over *Okumura* in view of the admitted prior art for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 17.

Claim 17 recites (emphasis added):

> 17. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:

> compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;
>
> store the first value in a first destination register of the processor ***when the first value is less than or equal to the second value***; and
>
> store the second value in the first destination register of the processor and an index value in a second destination register of the processor ***when the second value is less than the first value***, the index value representing the second source register.

While claims 1 and 17 are not coextensive in scope, Applicants rely on arguments similar to those expressed above for claim 1. Claim 17 recites a processor adapted to: 1) store the first value in a first destination register of the processor when the first value is less than or equal to the second value; and 2) store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is less than the first value. Based on a comparison between the first value and second value, the processor performs a certain action. If the first value is less than or equal to the second value, the processor stores the first value in a first destination value. If the second value is less than the first value, the processor stores the second value in the first destination register of the processor and an index value in a second destination register. *Okumura, at most, discloses one of the features but fails to disclose the other feature.* The Examiner relies on FIG. 3 of *Okumura* to teach these features. According to FIG. 3, step S9 is performed if register 5 is less than specific register 11. However, when specific register 11 is less than register 5, then *Okumura* only discloses that step S9 is not executed. (*See* related text for FIG. 3, *Okumura*.) *Okumura* fails to disclose a

processor adapted to take action under both conditions. Moreover, this feature is not disclosed by Applicants' admitted prior art.

Accordingly, Applicants respectfully submit that independent claim 17 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach or suggest the highlighted features in claim 17 above. Furthermore, Applicants submit that dependent claims 18-19 are allowable for at least the reason that these claims depend from an allowable independent claim.

C. Independent Claim 36

Applicants respectfully submit that independent claim 36 patently defines over *Okumura* in view of the admitted prior art for at least the reason that the combination fails to disclose, teach, or suggest the features emphasized below in claim 36.

Claim 36 recites:

> 36. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:
> compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;
> store the first value in a first destination register of the processor ***when the first value is greater than or equal to the second value***; and
> store the second value in the first destination register of the processor and an index value in a second destination register of the processor ***when the second value is greater than the first value***, the index value representing the second source register.

On page 10, the Office Action relies on the same arguments set forth in rejecting

claim 17 to reject claim 36. As set forth above for claim 17, *Okumura* fails to disclose a processor adapted to take action under both conditions (emphasized above). *Okumura*, at most, discloses one of the features but fails to disclose the other feature. Moreover, this feature is not disclosed by Applicants' admitted prior art. Accordingly, Applicants respectfully submit that independent claim 36 patently defines over *Okumura* for at least the reason that *Okumura* fails to disclose, teach, or suggest the highlighted features in claim 36 above. Furthermore, Applicants submit that dependent claims 37 and 38 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 50-0835.

Respectfully submitted,

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